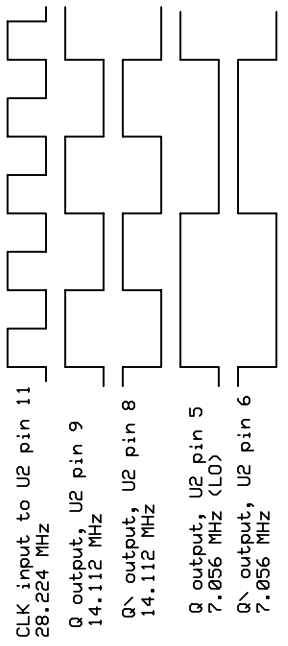


**Quadrature Sampling Detector Circuit (QSD)**

**QSD Timing Diagram**



CLK input to U2 pin 11  
 Q output, U2 pin 9  
 Q-bar output, U2 pin 8  
 Q output, U2 pin 5  
 Q-bar output, U2 pin 6  
 U3, S1 and S2 closed (integrate RF signal in C17, 0-90 degrees of LO)  
 U3, S1 and S3 closed (integrate RF signal in C16, 90-180 degrees of LO)  
 U3, S4 and S1 closed (integrate (-)RF signal in C17, 180-270 degrees of LO)  
 U3, S4 and S2 closed (integrate (-)RF signal in C16, 270-360 degrees of LO)

**FLEX RADIO FRIENDS**

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