Janus – a Sound Card designed for Software Defined Radios

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Abstract

The design, evolution and implementation of a sound card, Janus, targeted to amateur radio Software Defined Radio applications is discussed. The evaluation of a number of A/D converters considered for the design is also discussed. The Janus board is a high quality A/D and D/A converter board designed to work with amateur radio SDR applications. The card supports 24 bit sampling at 48, 96, and 192 khz sampling rates with performance exceeding consumer sound cards currently available on the market. The Janus board is designed to work with the HPSDR.org Atlas backplane and Ozymandias controller card.

Keywords

Software Defined Radio, SDR, HPSDR, Janus, Ozymandias

Introduction

One of the major determinants of the quality of a Software Defined Radio is the sound card used to digitize the IQ signals from the radio hardware. Additionally, a sound card with 4 input channels and 4 output channels is desired for an SDR in order to implement functions such as VOX and monitoring of transmitted audio or CW sidetone.

Many of the consumer and prosumer audio cards available on the market are quite good. The M Audio Delta 44 is probably the preferred sound card these days for SDR. It has 4 inputs and 4 outputs, 24 bit sampling at rates to 96 kHz. Unfortunately, it is only available as a PCI card, so it is not appropriate for a laptop computer. For a laptop the best alternative as of this writing is a Prosonus Firebox – a firewire attached device capable of 24 bit 96 kHz sampling.

The sound cards on the market today have some limitations when one tries to use them as A/D and D/A converters for SDR. None of the prosumer/consumer cards on the market today can sample greater than 96 kHz, and they often have filtering on the inputs and outputs that starts to roll off above 20 kHz. This is not desirable for an SDR. Another problem with the current sound cards is that there are none that are USB attached are capable of sampling above 48 kHz.

Given the compromises one makes using consumer/prosumer sound cards for SDR, in November of 2005 a number of SDR enthusiasts decided to design and build a sound card specifically for SDR applications. The goals of the board would be:

- 192 kHz, 24 bit sampling
- High S/N ratio – at least as good as the Delta 44
- Single connection to the computer - e.g. USB 2
- Full Duplex
- 4 input and 4 output channels to provide VOX, Sidetone and Monitor support

- Some extra IO to handle PTT and possibly RF hardware control

Basic Design

The basic design calls for an A/D converter for IQ and a D/A for transmit IQ, as well as A/D converter for microphone input and a D/A converter for received audio. Glue logic or a microcontroller is needed to interface to the various A/D and D/A converters.

Additionally a USB interface is needed to send the digitized data to the PC and to receive the processed audio from the PC to be sent to the D/A converters.

To meet our design goals a high quality A/D converter would be needed for digitizing IQ from the RF downconverter. After looking thru the specifications of many high end audio A/D chips, we decided to investigate the Wolfson WM8785, TI PCM 4202 and the Cirrus Logic CS 5381. All of these devices are 24 bit, 192 kHz sampling converters claiming a 110 db, or better, dynamic range.

We also needed an A/D converter for microphone input and a D/A and audio amplifier for audio out. The dynamic range, bit depth and sampling requirements on these converters are not as stringent so we chose the TLV320AIC23B, a highly integrated stereo audio codec with a built in headphone amplifier.

Block Diagram

The overall sound card block diagram is shown in Figure 1. The A/D converter provides 24 bit samples at a sample rate of 48, 96 or 192 kHz. The TLV320AIC23 provides the microphone A/D converter and D/A converters for stereo audio output. These both operate at a 48 kHz sampling rate and 16 bits.

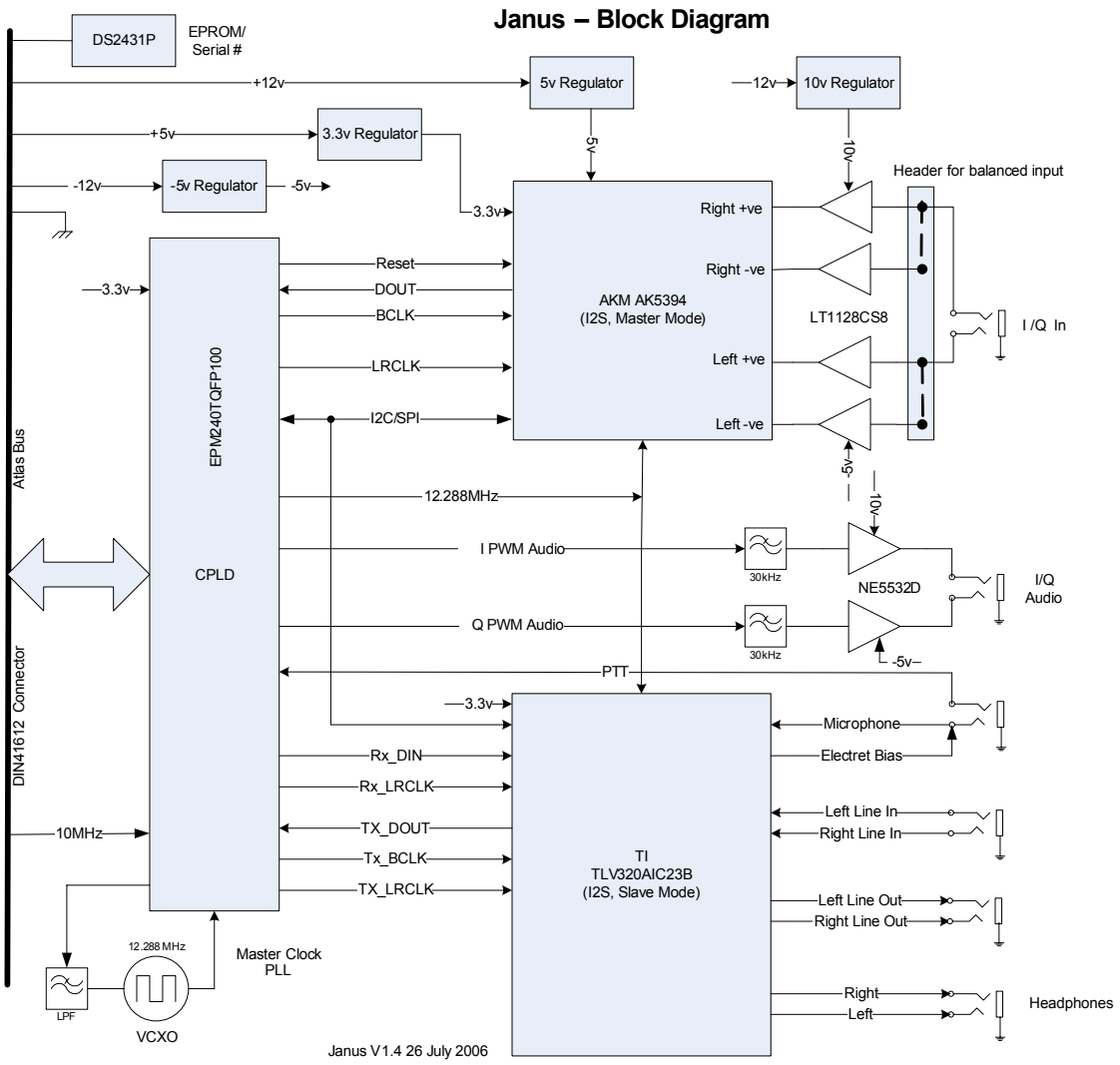

Figure 1 – Janus Block Diagram

For the D/A converters driving the I and Q outputs, a single bit over-sampling configuration was used. By sampling at 24MHz a simple Low Pass Filter is able to provide sufficient attenuation of the sampling frequency and minimize any phase difference between the two channels. The final design used a 16 bit single bit D/A converter implemented in an Altera FPGA.

In order to interface the A/D and D/A converters to a GUI based control program, running on a PC, a USB 2 interface was selected. USB 2 is specified to operate at 480Mbps. However, other experimenters using USB2 for a similar function [1] report being able to obtain a maximum combined (i.e. simultaneous input and output) transfer rate of 280Mbps.

The fastest transfer rate occurs from the Janus board to the PC. At a 192 kHz sampling rate this consist of

2 x 24 bit I/Q data plus 16 bit microphone data

which requires a sustained transfer rate of approximately 12Mbps, well within the practical rates reported by others.

There are a number of ways that the USB interface could have been implemented. We chose to use the Cypress FX2 family of devices. These provide a USB2 interface and an 8051 uP in the same chip. The device has been used successfully in a number of similar projects [1] and is well supported with open source code and development tools.

One design option would have been to use the 8051 uP to provide the interface to the various A/D and D/A converters as well as interfacing to the USB controller. However, it was considered that this may result in a bottleneck in the uP so instead the FX2 was used solely to provide the USB interface.

The Janus board forms part of the HPSDR (High Performance Software Defined Radio) project [2]. All boards plug into a standard backplane (called 'Atlas') that uses DIN41612 connectors.

The Janus was the first card to be designed following the design of the Atlas bus. At such an early stage in the development project it would have been very unwise to define, and fix, a considerable number of bus signals.

To provide total flexibility to the Janus pin definitions, and to enable multiple Janus boards to be connected to the Atlas bus, an Altera Max II CPLD was used for the interface.

The CPLD basically provides a software configurable 'patch panel' allowing any Janus signal pin to be connected to any signal pin on the Atlas bus. At $6 (qty 1) this is considered to be cheap insurance for pin assignments that will most certainly be altered in the future.

Design Considerations

Given the full duplex data requirements, and the desirability of parallel processing, an FPGA solution was selected to interface to the FX2 USB chip.

Prototype development was undertaken using an FPGA development board manufactured by Jean Nicolle (www.fpga4fun.com) called a Xylo board. This consists of an Altera Cyclone EP1C3T100 FPGA interfaced to an FX2 chip and provides a USB 2 interface to a PC.

PowerSDR was modified to use the Xylo interfaces for audio input and output. USB bulk transfer mode was used, the hope being that at USB 2 speeds (480 Mbps) isochronous mode would not be needed to achieve acceptable performance. This turned out to be correct and simplified initial development of code to talk to the early Janus prototypes.

The Xylo board comes complete with drivers, sample code and reduced the startup learning curve and risks considerably. Since neither of the authors had any prior experience with FPGA development, nor programming in an HDL, the use of the development board was highly successful and indeed very enjoyable.

We chose to program the FPGA in Verilog rather than schematic. Advice from those experienced in this art suggested that schematic design was easy for those with an electronics background but soon became unwieldy on larger designs.

We chose Verilog as our HDL since its syntax is very C like, which both Authors had previous experience in. The free Altera 'Quartus II' IDE was used for development and simulation and was found to be feature rich and a highly productive development environment.

The FPGA code was developed over a period of four months, additional features being added incrementally over previous versions. Given the geographic separation between the Authors, extensive use was made of the Internet to transfer 'work in progress' code between continents. In addition daily use of VoIP, in the form of TeamSpeak, helped to give the development a more personal feel.

A/D Converter Evaluation

Given the relatively simple requirements of the microphone A/D and audio D/A converters it was not felt necessary to evaluate more devices than the TLV320AIC23. Intended for the MP3 player mass market the device provides totally adequate performance at a very low price ($7.00 one off).

From the data sheets there appeared to be little to choose between the Wolfson WM8785, TI PCM 4202 and Cirrus Logic CS 5381 for the 24 bit A/D converter.

Initial design work was undertaken using the WM8785. This gave us the opportunity to develop an I2S type interface in the FPGA as well as leaning how to set up the chip via its I2C interface.

The screen shot at Figure 2 is that of an WM8785, operating at 48 kHz, connected to a Xylo FPGA development board over USB to the PowerSDR software [3].
The I and Q inputs to the WM8785 were provided by a Flex-Radio SDR1000 [4].

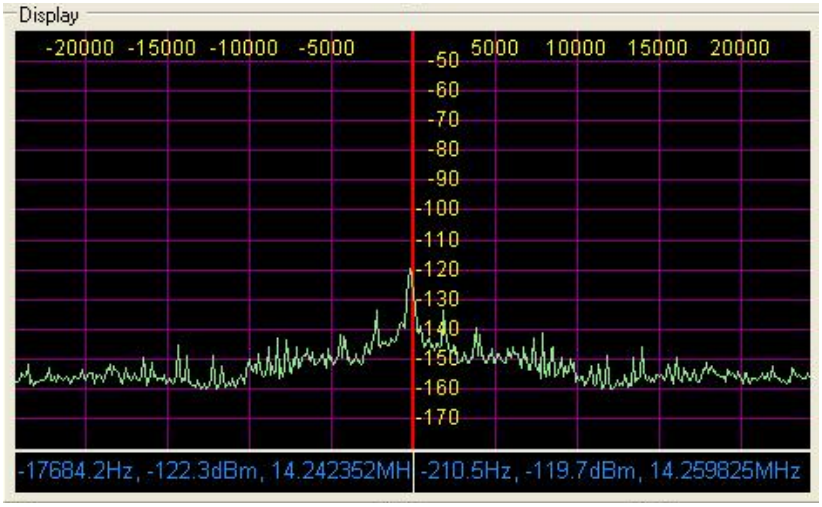

Figure 2 – WM8785 @ 48khz Sampling

The system was calibrated by connecting a 14MHz signal into the antenna socket at -50dBm. The I and Q inputs where then removed, the inputs shorted, and the noise level and spurious signals evaluated.

Note that although the overall system was calibrated the noise floor shown in Figure 2 does not represent that of the WM8785. This is due to the fact that the displayed value is reduced by 1dB for each dB of gain that the SDR1000 provides.

Whilst there may appear to be a large number of spurs close to 0 Hz, in practice, with the SDR1000 connected to an efficient antenna, these are mostly below the noise floor of the receiver.

Since future Software Defined Radio designs may wish to use a lower gain prior to the A/D converter it was decided to evaluate additional devices to see if a lower spur level could be obtained.

The TI PCM 4202 gave very similar results to the WM8785 and being somewhat easier to obtain, and cheaper, was considered for some time to be a likely candidate for the final design. However, the close-in spurs were still somewhat higher than desirable.

Figure 3 shows the results for a Cirrus Logic CS 5381. This had significantly lower close in spurs than the previous devices and was initially selected as the final candidate.

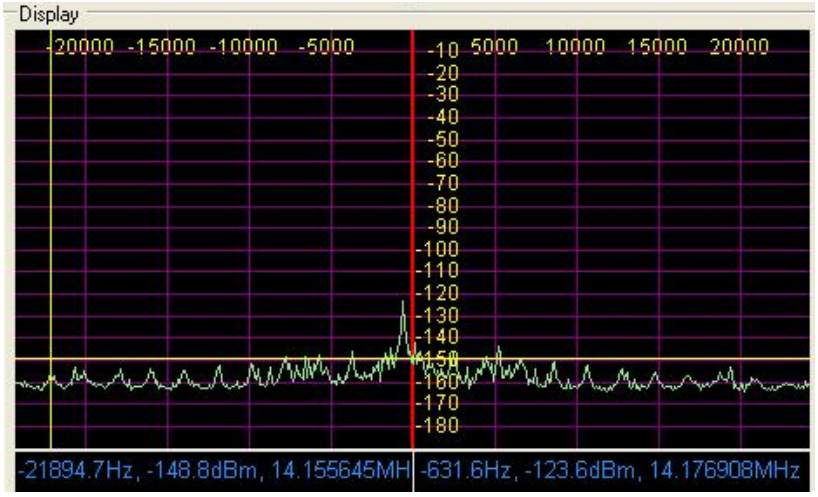

Figure 3 – Cirrus Logic CS5381 @ 48khz Sampling

High Sampling Rate Performance

The initial evaluation was done at 48 kHz sampling rate since this was easy to support in the FPGA and PowerSDR software. As our Verilog skills improved we modified the code to run at 96 kHz. Re-evaluating the previous devices at 96 kHz again confirmed the selection of the CS 5381 due its superior performance in relation to close in noise and spurs.

Initial circuit diagrams and PCB layouts were started in preparation for the development of a prototype board.

Prior to finalizing circuits and PCB design it was suggested by Bob McGwier, N4HY, that we should test the breadboards at 192 kHz since his prior experience with A/D converters indicated that there may be some issues at this speed.

Figures 4, 5 and 6 show the Wolfson, TI and Cirrus Logic chips respectively operating at 192 kHz sampling rate. As can be seen, Bob was correct to suggest we test at this sampling rate since all is not well!

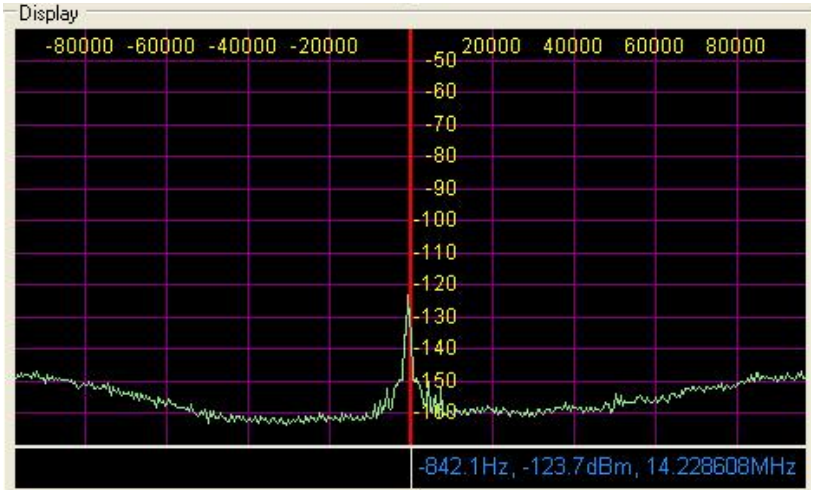

Figure 4 – Wolfson WM8785 @ 192khz sampling rate

Since these A/D converters are intended for use in the audio frequency range it would appear that the manufactures alias noise above this range in order to provide sampling at 192 kHz.

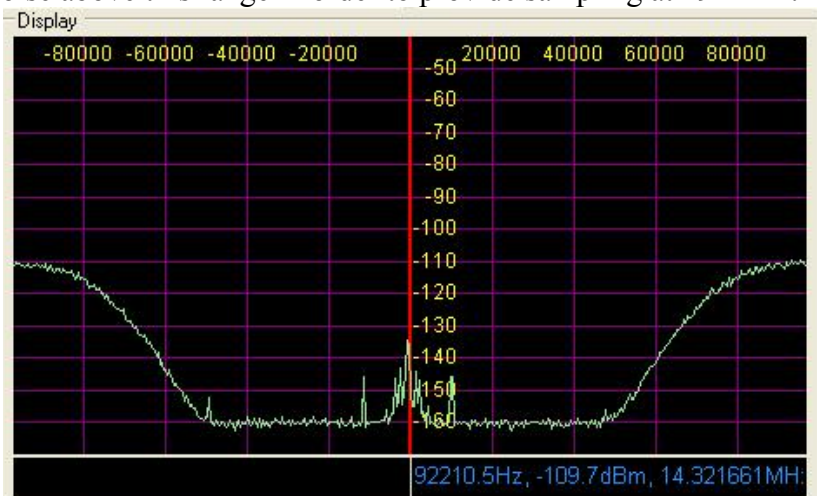

Figure 5 – TI PCM4202 @ 192khz Sampling

To be fair to the manufactures, should these devices be used for their intended purpose in the audio range then their performance would be quite acceptable. However, for SDR use the noise above +/- 48 kHz would intermodulate with band signals and render the receiver unusable.

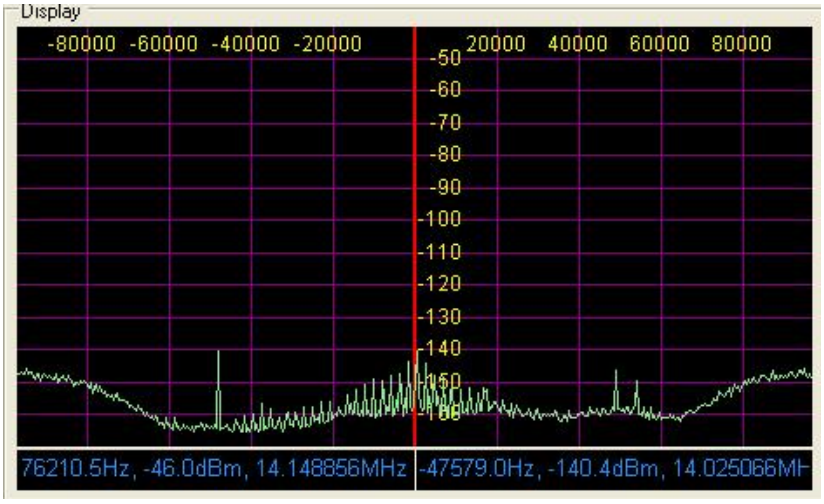

Figure 6 – Cirrus CS5381 @ 192 khz Sampling

Seeing these results Bob suggested we evaluate an AKM AK5394A. From the specifications this chip appeared to have similar performance to the CS 5381. The disadvantage was that it was that at $16 (qty 1) it was the most expensive of the devices so far evaluated and also rather difficult to source in evaluation quantities.

A few samples were rapidly obtained and shipped to Australia for VK6APH to evaluate. Figures 7, 8, and 9 show the AK5394A operating at 48, 96 and 192 kHz respectively.

Figure 7 – AK5394A @ 48 khz Sampling

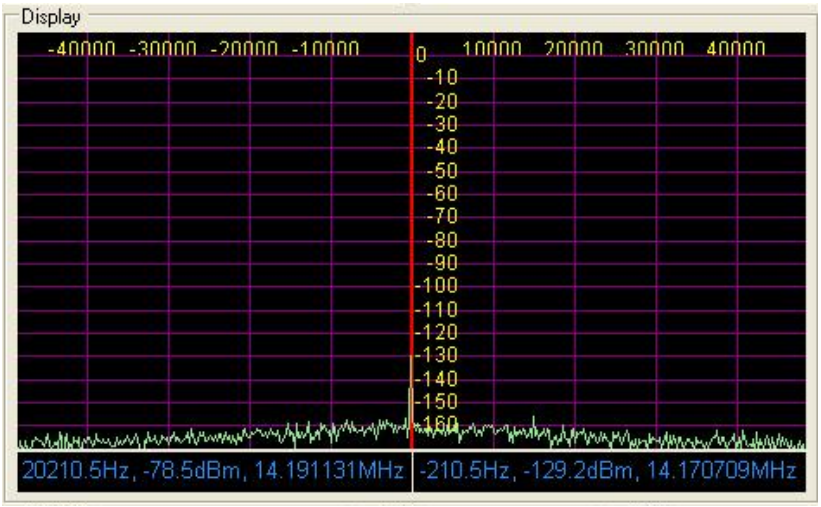

Figure 8 – AK5394A @ 96 khz Sampling

Not only was the previous aliasing problem at 192 kHz not present in this device but the close in noise and spurs were significantly lower. Needless to say the AK5394A was immediately selected as the A/D of choice for the Janus project!

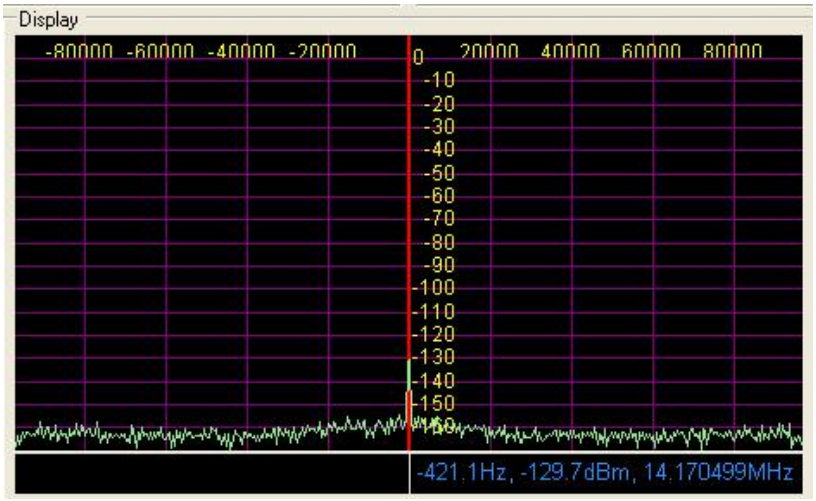

Figure 9 – AK5394A @ 192 khz Sampling

Production and Xylo replacement

With the selection of components completed, Lyle Johnson, KK7P, undertook the design of a suitable PCB. One issue that had come up in the breadboard prototype was that at 192 kHz the 48 kHz clock used for the TLV320 was visible in the noise floor. (This is not visible in Figure 9 since this image is of a PCB version of the circuit).

However, with careful layout, and separation of analogue and digital ground planes, Lyle was able to completely eliminate the clock pickup and achieve a noise floor equal to that of the breadboard prototype.

Whilst the Xylo FPGA was ideal for developing the code to interface the A/D and D/A converters to USB it did not provide sufficient spare input/output pins for all the facilities we required. Additionally the Cyclone EP1C3T100 FPGA on the Xylo is somewhat limited in the number of RAM bits it provides. We use the RAM bits in the FPGA primarily as FIFOs to buffer the data going to and from the PC and found we were a little short on FIFO space at 192 kHz sampling rates.

As mentioned previously, the Janus card is part of the open source software and hardware HPSDR (High Performance Software Defined Radio) project [2]. As part of the overall project an FPGA based – USB 2 interface card was required. Christened 'Ozymandias' (Ozy for short) this was designed and developed by Phil Covington, N8VB, and provides the necessary FPGA resources together with the requisite number of I/O pins required by the Atlas bus and sufficient RAM bits for buffer FIFOs.

Results and Current status

The performance of the alpha PCB version of the Janus card has met all our design requirements. At the level of performance realized with this design it is very difficult to actually quantify and measure them since access to suitable professional quality test equipment was not available. Measurements have been limited to comparing the S/N ratio, noise floor and dynamic range against the Delta 44 sound card.

In all respects Janus exceeds the already excellent performance of the Delta 44. Whilst the AK5394A is specified as a 24bit device in reality the ENOB is 20 bits. This is consistent with other professional sound cards. Whist this may be disappointing we should point out that some of the 16 bit sound cards that are built into PC motherboards yield an ENOB of only 12 bits!

A beta version of the Janus PCB is currently being constructed which will rectify a few minor errors on the alpha board. A new feature has been added to the beta board, namely the ability to phase lock the 12.288MHz Janus master clock to a 10MHz reference. This in turn may be locked to the 1pps from a GPS receiver.

This phase locking enables phase coherence of all oscillators in the HPSDR to be achieved.

A photo of a completed alpha Janus PCB is shown in Figure 10.

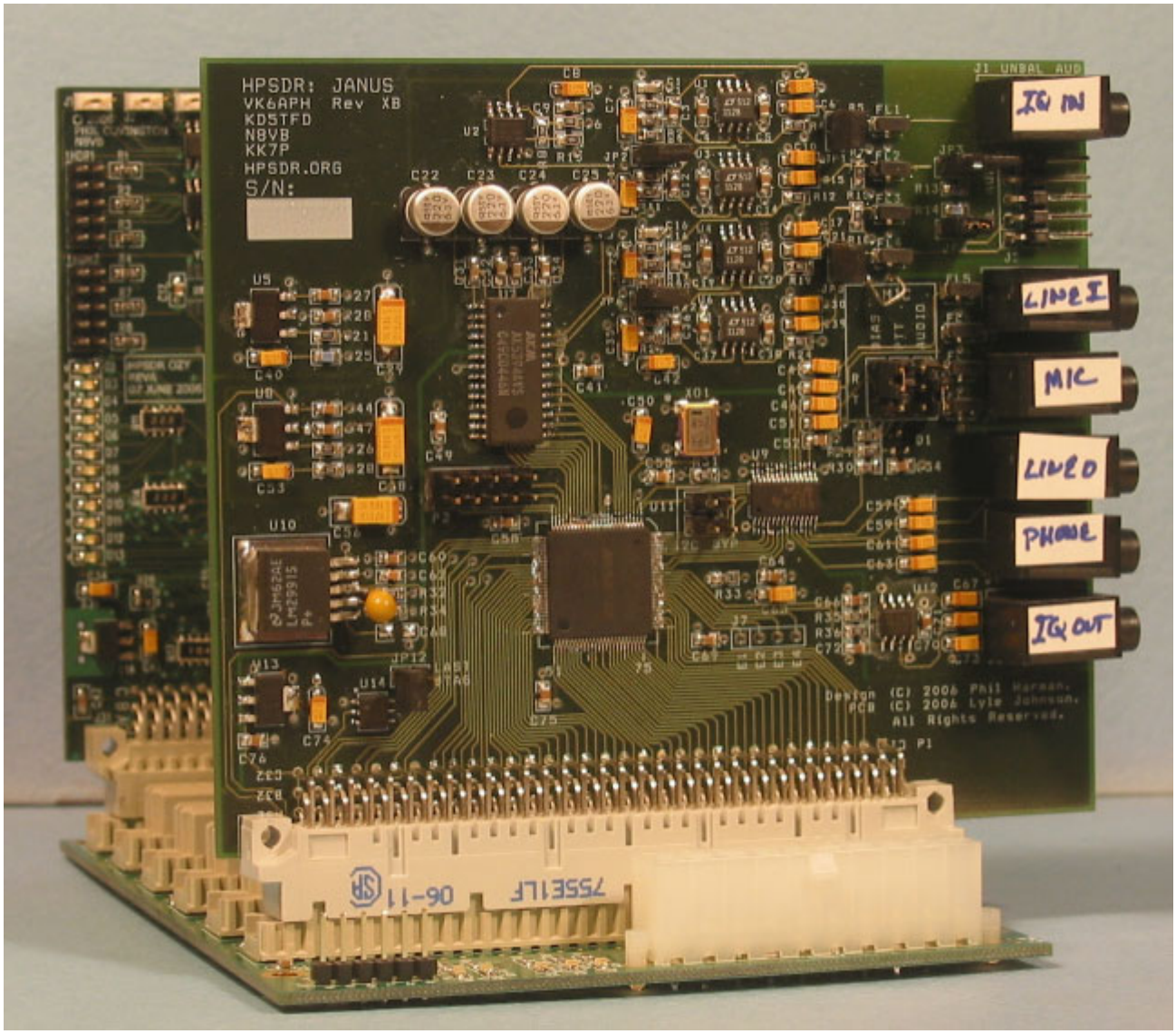

Figure 10 – Completed Janus prototype, mounted in Atlas backplane, Ozymandias board in background

Acknowledgements

The design of the Janus board was a collaborative effort by many of the members of the HPSDR reflector. The design issues were frequently discussed, and the authors actively supported and encouraged during the weekly "Flex-Radio Friends" TeamSpeak VoIP sessions.

The fact that a relatively complex design can be undertaken effectively with the two major developers living almost on opposite sides of the world is a tribute to the power of the Internet, the TeamSpeak forums and the active support of may interested hams.

There are many people that have contributed to the design of Janus, we would specifically like to thank Lyle Johnson, KK7P, Phil Covington, N8VB and Bob McGwier N4HY for their contributions.

References:

[1] GNU USRP project, see http://www.comsec.com/wiki?UniversalSoftwareRadioPeripheral
[2] Further details on the HPSDR can be found at hpsdr.org
[3] PowerSDR software and source code can be downloaded at http://www.flex-radio.com
[4] Further details regarding the SDR1000 are available at http://www.flex-radio.com